Amendments to the Claims:

Revise the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A power amplifier circuit comprising:

a scalable power amplifier including an output, and a plurality of selectively activated amplifier elements each operative to produce an RF output signal at the output, and operative to dynamically vary a power output level of the RF output signal in response to power output level data; [[and]]

a variable impedance circuit coupled to the output of the scalable power amplifier, and operatively responsive to the power output level data to vary an impedance of the variable impedance circuit to dynamically load the output of the scalable power amplifier; and

wherein the scalable power amplifier further includes an amplifier configuration circuit operatively responsive to the power output level data to selectively activate the selectively activated amplifier elements by at least reducing power to at least one of the selectively activated amplifier elements and wherein the variable impedance circuit further includes an impedance configuration circuit operatively responsive to the power output level data to dynamically vary the impedance of the variable impedance circuit.

2. (canceled)

PN 2 ~~3.~~ (original) The power amplifier circuit of claim ~~2~~ 1 wherein the amplifier configuration circuit provides a bias control signal to the scalable power amplifier to control a bias of the scalable power amplifier in response to the power output level data.

3 4. (original) The power amplifier circuit of claim 1 2 wherein the amplifier configuration circuit is operatively coupled to at least one of the amplifier elements to dynamically vary a bias level and a power output level of at least one of the amplifier elements in response to the power output level data.

1 4 5. (original) The power amplifier circuit of claim 2 wherein the variable impedance circuit includes at least one of resistive and reactive elements coupled via a switch to the output of the scalable power amplifier, and wherein the impedance configuration circuit activates the switch to vary the impedance of the variable impedance circuit and to dynamically load the output of the scalable power amplifier in response to the power output level data.

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5 6. (currently amended) A power amplifier circuit operative to receive an RF input signal and to produce an RF output signal comprising:

a device configuration circuit operatively responsive to power output level data to provide a device configuration signal and a variable load impedance signal;[[and,]]

a scalable power amplifier including an output, and a plurality of selectively activated amplifier elements, each operative to receive the RF input signal, and each operative to produce the RF output signal at the output wherein at least one of the selectively activated amplifier elements is operatively responsive to the corresponding device configuration signal to operate in at least one of the first power output level and the second power output level, to vary a power output level of the scalable power amplifier;

a variable impedance circuit also coupled to the output of the scalable power amplifier and operatively responsive to the variable load impedance signal received from the device

configuration circuit to provide a first impedance load at the output of the scalable power amplifier corresponding to the first power output level, and a second impedance load at the output of the scalable power amplifier corresponding to the second power output level; and

wherein each of the at least one of the plurality of selectively activated amplifier elements is operatively coupled to a first reference potential via a corresponding voltage supply switch wherein:

the corresponding voltage supply switch couples the first reference potential to the corresponding amplifier in response to a device configuration signal associated with the first power output level, and

the corresponding voltage supply switch reduces the first reference potential to the corresponding amplifier in response to a device configuration signal associated with the second power output level.

7. (canceled)

PN 6 ~~8.~~ (original) The power amplifier circuit of claim ~~7~~ 5 wherein the device configuration circuit produces a bias control signal, wherein each of the selectively activated amplifier elements includes an FET transistor having a gate operative to receive the RF input signal and the bias control signal via a reactive element, a drain operatively coupled to the output and to the corresponding voltage supply switch to receive the first reference potential in response to the device configuration signal, and a source operatively coupled to a second reference potential.

7 ~~9.~~ (original) The power amplifier circuit of claim 5 ~~7~~ wherein the at least one of the plurality of selectively activated amplifier elements that operates in the second power output level does not substantially receive the first reference potential.

8 ~~10.~~ (original) The power amplifier circuit of claim 6 ~~8~~ wherein each voltage supply switch includes at least one of an FET transistor including a gate operative to receive the device configuration signal, a drain operative to receive the first reference potential, a source operatively coupled to the drain of the corresponding parallel coupled amplifier, and a bipolar transistor including a base operative to receive the device configuration signal, a collector operative to receive the first reference potential, and an emitter operatively coupled to the drain of the corresponding parallel coupled amplifier.

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9 ~~11.~~ (original) The power amplifier circuit of claim 5 ~~7~~ wherein the at least one of the plurality of selectively activated amplifier elements transitions between the first power output level and the second power output level in at least one of a continuous manner and a discrete manner.

10 ~~12.~~ (currently amended) A power amplifier circuit operative to receive an RF input signal and to produce an RF output signal comprising:

a device configuration circuit operatively responsive to power output level data to provide a device configuration signal and a variable load impedance signal associated with a first and second power output level;

a scalable power amplifier having an output, and a plurality of selectively activated amplifier elements, each operative to receive the RF input signal via a corresponding RF input

switch, and each selectively activated amplifier element is operative to produce the RF output signal at the output of the scalable power amplifier, wherein at least one of the plurality of selectively activated amplifier elements is operatively responsive to the device configuration signal associated with the first power output level to receive the RF input signal from the corresponding RF input switch, wherein at least one of the plurality of selectively activated amplifier elements is operatively responsive to the device configuration signal associated with the second power output level to receive the RF input signal having a reduced amplitude from the corresponding RF input switch; [[and]]

a variable impedance circuit coupled to the output of the scalable power amplifier and operatively responsive to the variable load impedance signal to provide a first impedance load at the output of the scalable power amplifier associated with the first power output level, and a second impedance load at the output of the scalable power amplifier associated with the second power output level; and

a variable bias circuit operatively coupled to the device configuration circuit to receive bias control data and to responsively produce a bias control signal in response to bias control data to control a bias of at least one of the selectively activated amplifier elements.

11 ~~13.~~ (original) The power amplifier circuit of claim ~~12~~ 10, wherein each RF input switch switches the received RF input signal to the selectively activated amplifier elements in at least one of a continuous manner and a discrete manner.

14. (canceled)

12 ~~15.~~ (original) A wireless device comprising:

a processing circuit operative to produce power output level data;

a scalable power amplifier including an output, and a plurality of selectively activated amplifier elements each operative to produce an RF output signal at the output, and operative to dynamically vary a power output level in response to the power output level data;

a variable impedance circuit coupled to the output of the scalable power amplifier, and operatively responsive to the power output level data to vary an impedance of the variable impedance circuit to dynamically load the output of the scalable power amplifier; [[and]]

an antenna operatively coupled to the output of the scalable power amplifier and operative to transmit the RF output signal; and

wherein the scalable power amplifier further includes an amplifier configuration circuit operatively responsive to the power output level data to selectively activate the selectively activated amplifier elements by at least one of reducing power to at least one of the selectively activated amplifier elements and controlling a bias of at least one of the selectively activated amplifier elements, and wherein the variable impedance circuit further includes an impedance configuration circuit operatively responsive to the power output level data to dynamically vary the impedance of the variable impedance circuit.

16. (canceled)

13 ~~17~~. (original) The wireless device of claim ~~16~~ 12 wherein the device configuration circuit provides a bias control signal to the scalable power amplifier to control a bias of the scalable power amplifier in response to the power output level data.

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14 ~~18~~. (currently amended) An amplification method comprising:

selectively activating at least one selectively activated amplifier element within a scalable power amplifier including an output to vary a power output level of the scalable power amplifier; [[and]]

varying an impedance of a variable impedance circuit coupled to the output to dynamically load the scalable power amplifier by varying the impedance of the variable impedance circuit; and

wherein the selectively activated amplifier elements are selectively activated by at least one of reducing power to at least one of the selectively activated amplifier elements, increasing power to at least one of the selectively activated amplifier elements and controlling a bias of at least one of the selectively activated amplifier elements.

19. (canceled)

15 ~~20.~~ (original) The method of claim ~~18~~ 14 including providing a bias control signal to the at least selectively activated amplifier elements to control a bias of the plurality of selectively activated amplifier elements.

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16 ~~21.~~ (original) The method of claim ~~18~~ 14 comprising:

receiving an RF input signal by the scalable power amplifier, wherein each of the at least one selectively activated amplifier element receives the RF input signal; and

producing an RF output signal by the at least one selectively activated amplifier element.

17 ~~22.~~ (original) The method of claim ~~18~~ 14 comprising:

providing a first reference potential to the at least one selectively activated amplifier element, to operate in a first power output level in response to a device configuration signal associated with the first power output level; and

reducing a voltage from the first reference potential to the at least one selectively activated amplifier element to operate in a second power output level, in response to a device configuration signal associated with the second power output level.